

**IN THE SPECIFICATION:**

**Please revise the following paragraphs:**

**Page 5, paragraph [0020] to read as follows:**

--After forming gate dielectric 12 on a surface of semiconductor substrate 10, a plurality of gate regions stacks 14 are formed atop the layer of gate dielectric. As shown in Figure 1, each gate stack is comprised of two layers 20 and 22, one on top of the other. Preferably, the first layer 20 is comprised of intrinsic polycrystalline or so called poly silicon, and the second layer 22 is comprised of polycrystalline or so called poly germanium. Also, for example, each layer may be about 50 to 150 nm in height. The thicker the polySi layer, it is the more difficult it is to heavily dope the polySi near the gate dielectric 12 without degrading the S/D diffusion profile, since the higher energy implantation is required to heavily dope the polySi near the gate dielectric. The gate stack 14 is positioned by using conventional lithography and etching steps. The photoresist used is stripped after the etch to form the gate stack structure shown in Figure 1.—

**Page 6, paragraph [23] to read as follows:**

-- With reference to Figure 2, after gate stack 14 is formed, an oxide/nitride line 24 is deposited on the stack and on the semiconductor substrate 10 immediately around the gate stack. After this, an oxide, disposable space 26 is formed around the gate stack 14 by conformally depositing the oxide and directionally etching the oxide by reactive ion etching (RIE). The RIE removes the layers liner 24 and spacer 26 from the top of the gate stack 14 and the exposed Si substrate area. The disposable layer 22, of at least the same thickness as, or thicker than, that of polySi layer 20, is was added and the at least 2x fatter space 26 is was formed so that the deep polySi doping implantation (discussed below) is kept away from the critical region of S/D diffusion near the extension.--

**Page 6, paragraph [24] to read as follows:**

-- With reference to ~~Figure Figures 2 and 3~~, the disposable poly Ge layer 22 is removed from ~~gate~~ stack 14; and this may be done, for example, by a  $H_2O_2$  or  $HNO_3$  etching process, while the PFET area is covered by a photo resist. After the poly Ge layer is removed, an ~~as~~ As or P deep ion implantation process 100 is employed to dope the N<sup>+</sup> polySi ~~gate~~ layer 20. The implant goes into the substrate 10, ~~forming extension regions 30~~, but it is kept sufficiently away from the active device area by the fat spacer 26. ~~After the N<sup>+</sup> polySi gate implantation is performed, the NFET area is then covered by photoresist, poly Ge 22 is removed and Boron deep implantation is performed to dope the P<sup>+</sup> polySi gate 20 (not shown).~~ --

**Page 6, paragraph [26] to read as follows:**

-- With reference to Figure 5, after the n<sup>+</sup> and p<sup>+</sup> extension implantation, n<sup>+</sup> and p<sup>+</sup> source/drain diffusion regions 30 are doped by ion implantation 104 with the third spacer 40 formed over spacer 36 and with using blocking photoresist mask (not shown in the Figure). --